UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/088,674	06/02/1998	DANIEL J. MORGAN	TI-25995	2025

23494 7590 03/12/2008

TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
NGUYEN, KEVIN M	

ART UNIT	PAPER NUMBER
2629	

NOTIFICATION DATE	DELIVERY MODE
03/12/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

uspto@ti.com
uspto@dlemail.itg.ti.com

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte DANIEL J. MORGAN GREGORY J. HEWLETT and PETER F. VANKESSEL

Appeal 2007-3586
Application 09/088,674[1]
Technology Center 2600

Decided: March 10, 2008

Before JAMESON LEE, RICHARD TORCZON and SALLY C. MEDLEY, *Administrative Patent Judges*.

MEDLEY, *Administrative Patent Judge*.

DECISION ON APPEAL

---

[1] Application filed on 02 June 1998. The real party in interest is Texas Instruments Incorporated.

A. Statement of the Case

This is an appeal under 35 U.S.C. § 134 from the Examiner's Final Rejection of claims 1-10. We have jurisdiction under 35 U.S.C. § 6(b). We reverse.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Aras	US 5,731,802	03/24/1998
Yamaguchi	US 6,222,515	04/24/2001

Claims 1-3, 5-8 and 10 stand rejected under 35 U.S.C. § 102(e) as anticipated by Yamaguchi.

Claims 4 and 9 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Yamaguchi and Aras.

BACKGROUND

The invention is related to a method and system for providing boundary dispersion to pixel values displayed on a binary spatial light modulator (SLM) to reduce temporal contouring artifacts. Pixel code values are offset from a nominal pixel value when displayed on the SLM to disperse a large bit transition for a pulse width modulation (PWM) system. Nominal pixel values are offset alternately between a positive offset and a negative offset, repeatedly over a sequence of two displayed frames, where the average value of the two offset values over two displayed frames as seen by the viewer is equal to the nominal pixel value. The offset varies as a function of the nominal pixel value, the pixel spatial location on the screen, and pixel temporal location in time. (Spec. 3-4 and 6-8, Abs. and fig. 2).

B. Issues

The fist issue before us is whether the Examiner erred in determining that claims 1-3, 5-8 and 10 are anticipated under 35 U.S.C. § 102(e) by Yamaguchi?

The second issue before us is whether the Examiner erred in determining that claims 4 and 9 are unpatentable 35 U.S.C. § 103(a) over Yamaguchi and Aras?

For the reasons that follow, the Examiner has erred in determining that claims 1-3, 5-8 and 10 are anticipated under 35 U.S.C. § 102(e) by Yamaguchi and claims 4 and 9 are unpatentable 35 U.S.C. § 103(a) over Yamaguchi and Aras.

C. Finding of Facts ("FF")

The record supports the following finding of facts as well as any other findings of fact set forth in this opinion by at least a preponderance of the evidence.

1. Applicants' claims 1-10 are the subject of this appeal.
2. Claims 1 and 6 are independent claims.
3. Claims 2-5 and 7-10 are dependent on claims 1 and 6 respectively.
4. Claims 1 and 6, 2 and 7, 3 and 8, 4 and 9, and 5 and 10 respectively stand or fall together since Applicants made identical arguments for each group.
5. Claims 1 and 6 are as follows:

> 1. A method of displaying digital video data comprising pixel values, said method comprising the steps of:
> offsetting a first pixel value a first predetermined amount to form a first offset pixel value and displaying said first offset pixel value during a first display frame; and

offsetting said first pixel value by the opposite of said first predetermined amount to form a second offset pixel value and displaying said second offset pixel value during a second display frame, such that the average of said displayed first offset pixel value and said second offset pixel value is said first pixel value.

6. A system of displaying digital video data comprising pixel values, comprising:

a logic circuit offsetting a first pixel value a first predetermined amount to form a first offset pixel value, said logic circuit also offsetting said first said pixel value by the opposite of said first predetermined amount to form a second offset pixel value; and

display means displaying said first offset pixel value during a first display frame and displaying said second offset pixel value during a second display frame, such that the average of said displayed first offset pixel value and said second offset pixel value is said first pixel value.

6. The Examiner found that Yamaguchi describes a system of displaying digital video data associated with a method comprising: a first pixel value of 3V mean effective voltage, where Yamaguchi inherently describes a first predetermined amount of -1V to form a first pixel offset value of 2 V, and displaying the first offset pixel during a first frame period; where Yamaguchi inherently describes an opposite of said predetermined amount of +1V to form a second offset pixel value of 4V and displaying the second offset pixel during a second frame period; and the average of the displayed first offset pixel value of 2V and said second offset pixel value of 4V is the first pixel value of 3V (Yamaguchi fig. 7B and col. 8, lines 11-27, Ans. 3-4 and Final Rejection 2-3).

7. Yamaguchi describes that data signals inputted to the data drivers **8** are used to select data voltages from the first and second liquid crystal

driving sources **16** and **17** to be applied to the data drivers **8** (col. 7, ll. 62- col. 8, ll.3, **figs. 1a-ab**).

8. Yamaguchi describes that a data driver for a liquid crystal that is able to simultaneously provide two voltage levels is employed to display 64 colors with 4 gray scale levels (col. 8, ll. 4-10).

9. Yamaguchi describes that an intermediate gray scale level (level 2) between two gray scale levels (levels 1 and 3) is realized by the mean effective voltage of 3V that results from the application of 2V (-1V) to the first field of the frame and the application of 4V (+1V) to the second field of the frame (col. 8, ll. 11-34, figs. 7A-7D).

D. Principles of Law

"Anticipation under 35 U.S.C. § 102(e) requires that 'each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.'" *In re Robertson*, 169 F.3d. 743 (Fed. Cir. 1999) (citing *Verdegaal Bros., Inc. v. Union Oil Co.,* 814 F.2d 628, 631 (Fed.Cir.1987).

E. Analysis

Claims 1 and 6

Claims 1 and 6 recite the limitations "displaying said first offset pixel value during a first display frame" and "displaying said second offset pixel value during a second display frame". The Examiner found that Yamaguchi describes a system of displaying digital video data associated with a method comprising: a first pixel value of 3V mean effective voltage where Yamaguchi inherently describes a first predetermined amount of -1V to form a first pixel offset value of 2V, and displaying the first offset pixel during a first frame period; where Yamaguchi inherently describes an opposite of said predetermined amount of +1V to form a second offset pixel value of 4

V and displaying the second offset pixel during a second frame period; and the average of the displayed first offset pixel value of 2V and said second offset pixel value of 4V is the first pixel value of 3V (FF[2] 6). The Examiner found the voltages of 2V and 4V described in Yamaguchi as the claimed offset pixel values. However, the Examiner has not explained how Yamaguchi describes that the two voltages (i.e. offset pixel values) are displayed as required by claims 1 and 6. According to Yamaguchi, the voltage values (i.e. 2V and 4V) are used to drive the pixels of an LCD panel to display the correct gray level (FFs 7-9). Thus, it is the color and gray level of the pixels that are displayed, not the voltage values. Furthermore, that a "pixel" is displayed as asserted by the Examiner (FF 6) is of no moment since claims 1 and 6 require displaying "pixel values" not just pixels. "[T]he name of the game is the claim."[3] "Anticipation under 35 U.S.C. § 102(e) requires that 'each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.'" Since the Examiner has failed to demonstrate that what he regards as pixel values in Yamaguchi are displayed, Claim 1 is not anticipated by Yamaguchi.

Claims 2-3, 5, 7-8 and 10

Since claims 2-3, 5, 7-8 and 10 include all the limitations of claims 1 and 6, for the same reasons as explained above, the Examiner has erred in determining that claims 2-3, 5, 7-8 and 10 are anticipated under 35 U.S.C. § 102(e).

[2] FF denotes finding of fact.
[3] *In re Hiniker Co.*, 150 F.3d 1362, 1369 (Fed. Cir. 1998).

Claims 4 and 9

Since claims 4 and 9 include all the limitations of claims 1 and 6, for the same reasons as explained above, the Examiner has erred in determining that claims 4 and 9 are unpatentable 35 U.S.C. § 103(a) over Yamaguchi and Aras.

Decision

Upon consideration of the record, and for the reasons given, the Examiner's rejections of claims 1-3, 5-8 and 10 as anticipated under 35 U.S.C. § 102(e) by Yamaguchi and claims 4 and 9 as unpatentable 35 U.S.C. § 103(a) over Yamaguchi and Aras are reversed.

REVERSED

Appeal 2007-3586
Application 09/088,674

MAT

TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS TX 75265